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10/765,662	01/27/2004	Takashi Tanimoto	81784.0299	9835

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EXAMINER	
KHOKHAR, ASIF I	
ART UNIT	**PAPER NUMBER**
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,662	TANIMOTO, TAKASHI	
	Examiner	Art Unit	
	Asif Khokhar	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Applicant's arguments filed 08/20/2007 have been fully considered but they are not persuasive.

With regard to claim 1, Applicant argues that " The cited reference fail to disclose a register that stores first and second setting data for designating driving conditions for first and second solid image capturing element." Page 5, paragraph 1. In response to the arguments, the examiner notes that applicant did not specify a particular type of register. Prior art discloses a memory, which stores data and register values. Memory inherently contains registers to store values. Furthermore, memory is capable to designate the driving conditions as explained in prior art (the control unit stores the first and second set time into memory 109, page 3, paragraph 2. Set time is a driving condition and since control unit 109 stores set time in memory, memory designates the set time, driving condition, to first and second image capturing element.)

For the reason above, the rejection is repeated.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

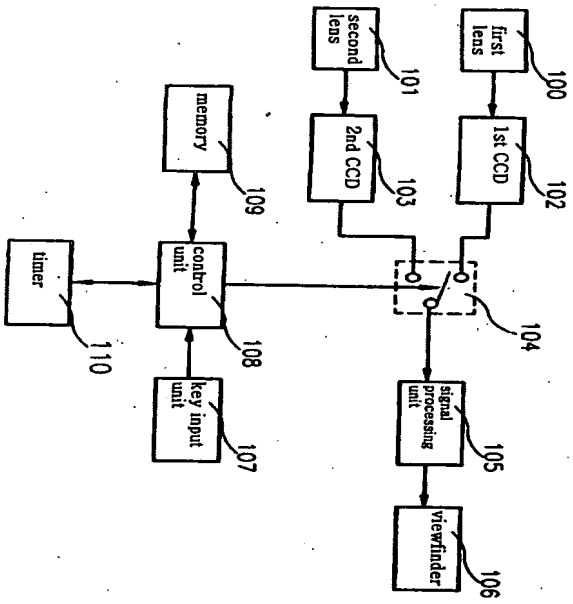
Claim 1 and 2 rejected under 35 U.S.C. 102(b) as being anticipated by Soon-Hun KR 1999-005761 (translation).

Regarding claim 1, Soon-Hun disclosed a video camera in Fig 1, which comprises the image capturing device (a camcorder, Abstract line 1) a first solid image capturing element

having a first plurality of light receiving pixels, for storing information charge which is generated in response to a first object image, in the first plurality of light receiving pixels (first lens 100 and 1st CCD 102, page 3, paragraph 2) a second solid image capturing element having a second plurality of light receiving pixels, for storing information charge which is generated in response to a second object image, in the second plurality of light receiving pixels (second lens 101 and 2nd CCD 103, page 3, paragraph 2) a driving control circuit for controlling operation of the first and second solid image capturing elements (control unit 108, page 3, paragraph 2) and a register for storing first and second setting data which respectively designate driving condition for the first and second solid image capturing elements (memory 109, page 3, paragraph 2) wherein the driving control circuit drives the first and second solid image capturing elements respectively according to the first and second setting data stored in the register (If the user sets the switching time of the first and second lens through the key input unit 109, the control unit 108 stores the first and second set time into memory 109, and when the user begins to take pictures, it checks the time of the timer 110 to control the switching unit 104. the switching unit 104 is a mean for switching between the output signal of the first and second CCD driving units 102 and 103 in accordance with the control of the control unit 108. Page 3, paragraph 2, line 11).

Drawing

Fig. 1



Regarding claim 2, Soon-Hun disclosed a video camera in Fig 1, which comprises the register comprises a memory region sectioned into a plurality of blocks for respectively storing the first and second setting data (The turnover time setup procedure (S100 ~ S105) is the process of setting up the display time of the first optic and being made of the first turnover time configuration stage (S100, S101, S102) stored in the memory, and the second turnover time configuration stage (S103, S104, S105). The second turnover time configuration stage (S103, S104, S105) sets up the display time of the second lens and stored in the memory, page 3, paragraph 5, line 1. A memory inherently sectioned into a plurality of blocks).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Soon-Hun KR 1999-005761 in view of Minakami US20010055064.

Regarding claim 3, Soon-Hun has been discussed above and the following:

The controller (108) is the means which checks the time of the timer (110) if a user stored the first and the second setup time in the memory (109) if a user set up the first, and the turnover time of the second lens through the key input part (107) and the photography starts and controls the switching unit (104), but doesn't disclose:

The driving control circuit comprises a timing control circuit for determining timing for conducting vertical and horizontal scanning relative to the first and second solid image capturing elements and generating a first timing signal and a second timing signal, a first driving circuit for driving the first solid image capturing element in response to the first timing signal, and a second driving circuit for driving the second solid image capturing element in response to the second timing signal, and the first driving circuit and second driving circuit are constructed such that driving capabilities thereof are respectively switchable and driving capabilities thereof to be employed are determined according to the first and second setting data, respectively.

Minakami '064 discloses the digital still camera, which is provided with an AF/AE/Zoom logic circuit 115 for controlling the optical mechanism system, a V driver 111, an H driver 112, and a timing signal generating circuit (TG/SSG) 113, for driving the CCD. FIG. 4 only shows one V driver, one H driver, and one TG/SSG for convenience. A set of the drivers and TG/SSG corresponding to each of the CCDs are present so as to drive the two CCDs 136, 105 (page 4, paragraph 57, line 1). The construction example of the digital camera of this embodiment is provided with a CCD signal process block 122 for color processing an image signal output from the A/D converter 108. This has a circuit construction which can color-process image data having different resolutions from the two CCDs in one process circuit where possible. For example, in the process of the CCD signal process block 122, a color separation process circuit, high frequency enhancement process circuit, .gamma. process circuit and the like have different horizontal and vertical synchronizing signals to be inputted, and the circuits can be shared. When the CCD signal process block 122 processes an image signal from the sub CCD 136, its color signal output is outputted to the main digital bus 135 and at the same time, can be directly transmitted through a two-way digital bus 143 to the logic process portion 115 corresponding to autofocus, photometry process, zoom process or the like (page 4, paragraph 61, line 1). The driving method therefor is as follows. During one screen, a light is irradiated onto the photosensitive portion 201 to accumulate signal electric charges. Upon completion of this, the signal electric charges are transferred to the light-shielded vertical CCD 202 provided between the photosensitive portions 201. The signal electric charges on the vertical CCD 202 are transferred to the horizontal CCD 203 provided in the lower portion (page 1, paragraph 5, line 5). For the purpose of this examination, the examiner considers AF/AE/Zoom logic circuit 115 as a

driving control circuit, which also controls the timing signal generating circuit (TG/SSG) 113. These circuits are shared in only one logic circuit in a range to be realized, to reduce the circuit size.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Soon-Hun KR 1999-005761 in the teaching of the Minakami '064 in order to determining time for conducting vertical and horizontal scanning relative to the first and second solid image capturing elements an generating a first timing signal and a second timing signal with driving control circuit comprising a timing control circuit. It will reduce the size of the circuit and the cost.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minakami '064 and Soon-Hun '761 in view of Ito US6275262. Minakami '064 and Soon-Hun '761 discussed above, but doesn't discloses:

A counter for counting a predetermined reference clock, a decoder for decoding an output from the counter to thereby create the first timing signal and the second timing signal, and a delay circuit for delaying the first timing signal and the second timing signal by a period of time which is changeable, wherein the delay circuit determines the period of time by which to delay, according to the first and second setting data.

Ito US6275262 discloses the imaging block 2 further has a timing signal generating circuit 24 for generating a VD signal, an HD signal and a CLK signal each serving as a basic clock used for operation of each of circuits in the video camera apparatus based on a reference clock from a reference clock circuit provided therein, and a CCD drive circuit 25 for supplying a

drive clock to the imaging device 22R, the imaging device 22G and the imaging device 22B based on the VD signal, the HD signal and the CLK signal supplied from the timing signal generating circuit. The VD signal is a clock signal representing one vertical period. The HD signal is a clock signal representing one horizontal period The CLK signal is a clock signal representing one pixel clock. The timing clock formed of these VD, HD and CLK signals is supplied to each of the circuits in the video camera apparatus through the CPU 4, though not shown (column 3, line 66). For examining purpose, examiner considers reference clock circuit as a counter. Timing signal generating circuit 24 generates a VD signal, an HD signal and a CLK signal each serving as a basic clock used for operation of each of circuits in the video camera apparatus based on a reference clock from a reference clock circuit provided therein, which is same as decoder. VD signal and HD signal performing the same function described by delay circuit. It further benefits the video camera apparatus for subjecting the video signals (R), (G), (B) to a predetermined signal processing.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the image capturing device invented by Soon-Hun in view of Minakami '064 in the teaching of Ito '262 to comprise a counter, decoder and a delay circuit to create the timing signals because the delay circuit improves the system speed.

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asif Khokhar whose telephone number is (571) 270-3221. The examiner can normally be reached on Monday- Friday 7:30am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan HO can be reached on (571) 272-7365. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TUAN HO
PRIMARY EXAMINER